Attorney's Docket No. 5308-168 PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re: Das et al.
Serial No.: 09/878,442
Filed: June 11, 2001
For: HIGH VOLTAGE, HIGH TEMPERATURE CAPACITOR AND INTERCONNECTION STRUCTURES

Group Art Unit: 2815
Confirmation No.: 2584
Examiner: J. Jackson, Jr.

Date: February 2, 2005

Mail Stop Issue Fee
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

PETITION TO ACKNOWLEDGE AND CONSIDER PREVIOUSLY FILED INFORMATION DISCLOSURE STATEMENT

Sir:

Applicants submitted an Information Disclosure Statement and Form PTO-1449 listing 3 cited references on January 27, 2005. Copies of the IDS cover sheet, Form PTO-1449, and the non-patent reference are attached as Appendix A. Also attached is a copy of the Auto-Reply Facsmile Transmission indicating receipt of the IDS by the U.S. Patent and Trademark Office on January 27, 2005. A Notice of Allowance for the present case was mailed on January 31, 2005. Thus, the Information Disclosure Statement dated January 27, 2005 was filed before the mailing date of the Notice of Allowance.

In light of the foregoing, Applicants request consideration of the Information Disclosure Statement of January 27, 2005, and return of an initialed form PTO-1449 indicating consideration of the Information Disclosure Statement of January 27, 2005.

It is not believed that a fee is due for the present petition; however the Commissioner is authorized to charge Deposit Account No. 50-0220 in the event that a fee is necessary to allow consideration of this paper.

Respectfully submitted,

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Traci A. Brown

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Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT UNDER 37 C.F.R. § 1.97(b)

Sir:

Attached is a list of documents on Form PTO-1449. A copy of any listed U.S. patent and/or U.S. patent application publication is not provided herewith in accordance with the amendment by the U.S. Patent and Trademark Office to 37 C.F.R. § 1.98(a)(2)(ii) effective October 21, 2004. It is requested that these documents be considered by the Examiner and officially made of record in accordance with the provisions of 37 C.F.R. § 1.56 and Section 609 of the MPEP.

This Information Disclosure is submitted in accordance with 37 C.F.R. § 1.97(b)(4), after the filing of a Request for Continued Examination under 37 C.F.R. § 1.114. Therefore, no fee is believed due. However, the Commissioner is hereby authorized to charge any deficiency or credit any overpayment to Deposit Account No. 50-0220.

Respectfully submitted,

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Traci A. Brown

FORM PTO-1449 U.S. Department of Commerce Patent and Trademark Office LIST OF DOCUMENTS CITED BY APPLICANT (Use several sheets if necessary)	Attorney Docket Number 5308-168	Serial No. 09/878,442
	Applicants: Das et al.	
	Filing Date: June 11, 2001	Group: 2815

U. S. PATENT DOCUMENTS

Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date if Appropriate
	1	6,767,843	7/2004	Lipkin et al.	438	758	
	2	6,342,748	1/2002	Nakamura et al.	310	313A	

FOREIGN PATENT DOCUMENTS

		Document Number	Date	Country	Class	Subclass	Translation
	3	JP 2000-252461A	9/14/00	Japan			**JPO Computer Translation**

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

EXAMINER _____ DATE CONSIDERED

*EXAMINER Initial if reference considered, whether or not citation is in conformance with MPEP 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

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DETAILED DESCRIPTION

[Detailed Description of the Invention]

[0001]

[Industrial Application] This invention relates to the manufacture method of the semiconductor device in which the low good gate insulator layer and silicon-carbide interface of interface level density were formed, in a semiconductor device, a semiconductor integrated circuit, etc. which carried the metal-oxide-film-semiconductor (MOS) structure where the silicon carbide was used as a semiconductor, or the MOS electric field effect type transistor.

[0002]

[Description of the Prior Art] The interface level density generated in the gate insulator layer / silicon-carbide interface which is a wide gap semiconductor, and which was formed on the silicon-carbide substrate (SiC substrate) is high 1 or more figures, and has become one of the causes of low channel mobility from the interface level density which generates a silicon substrate in the gate oxide film / silicon interface which oxidized thermally and was formed.

[0003] Moreover, it is with the MOS capacitor usually produced using the silicon substrate. Although the interface level density generated in a gate oxide film / silicon interface by carrying out hydrogen annealing at 400 degrees C, and carrying out termination of the dangling bond is reduced and it is made form a good interface, even if it carries out annealing at 400 degrees C with the MOS capacitor produced using the silicon-carbide substrate, there is no conspicuous effect which reduces the interface level density generated in a gate insulator layer / silicon-carbide interface.

[0004]

[Problem(s) to be Solved by the Invention] Then, termination of the uncombined hand of the silicon or carbon followed and kicked to the MOS capacitor interface produced using the silicon-carbide substrate in this invention is carried out, and it aims at forming a good interface with low interface level density.

[0005] In order to solve the above technical problem, invention-in-this-application persons found out wholeheartedly that the MOS capacitor of interface level density was obtained by annealing the MOS capacitor produced using the silicon-carbide substrate in the atmosphere containing the hydrogen under an elevated temperature as a result of research.

[0006]

[Means for Solving the Problem] This invention proposes the manufacture method of a semiconductor device of annealing in the atmosphere which contained hydrogen in 600-1600 degrees C, after forming more than two-layer [of an oxide film and/, or a nitride / one layer or two-layer] as a gate insulator layer on the semiconductor substrate which has a silicon carbide in the best layer at least based on the above-mentioned knowledge.

[0007] In addition, although there are very many polytypes, such as 3 C-SiC, 4 H-SiC, 6 H-SiC, and 15 R-SiC, in a silicon carbide (SiC), as long as the silicon carbide used as a semiconductor substrate in this invention is SiC, the thing of which type is sufficient as it.

[0008] Moreover, as long as the best layer is SiC, the structure which has 3 C-SiC on Si, and the structure which has 3 C-SiC on 6 H-SiC or 4 H-SiC are sufficient as the structure of a semiconductor substrate.

[0009] As an oxide film or a nitride, although a silicon oxide or a silicon nitride is common, which oxide film or nitrides, such as an aluminum oxide film, a tantalic-acid-ized film, an alumimium nitride film produced on another conditions, and a gallium nitride, are sufficient, without being limited to this.

[0010] As a method of carrying out the laminating of the oxide film on a silicon-carbide substrate, although an oxide film may be formed by the forming-membranes method on a silicon-carbide substrate, a silicon-carbide substrate may be oxidized thermally and an oxide film may be formed.

[0011] When forming a silicon oxide on a silicon-carbide substrate by the forming-membranes method, for example, after forming silicon on a silicon-carbide substrate by the MBE method (the Molecular beam epitaxy method) or CVD (chemistry gaseous-phase method), you may oxidize thermally and form and a silicon oxide may be formed by CVD and the SOG method (the spin on glass method).

[0012] On the other hand, as a method of carrying out the laminating of the nitride, the LPCVD method (low voltage chemistry gaseous-phase method) and plasma nitriding are employable on a silicon-carbide substrate.

[0013]

[Function] That is, after forming the gate insulator layer which consists of an oxide film or a nitride on a silicon-carbide (SiC) substrate, by annealing in the atmosphere containing 600 degrees C - 1600 degrees C hydrogen, termination of the dangling bond of the silicon which exists in an insulator layer / silicon-carbide interface, or carbon can be carried out, it can reduce interface

level density, and can form a good interface.
[0014] Since the melting point of the silicon oxide which the termination of the dangling bond of the silicon which exists in a gate insulator layer / silicon-carbide interface, or carbon is not fully made, and is used as for example, a gate insulator layer was 1600 degrees C when annealing below 600 degrees C, the annealing temperature was made into the range of 600 degrees C - 1600 degrees C.
[0015] Moreover, the hydrogen pressure force in the case of hydrogen annealing is at 0.1Pa or less. since there is no effect it is too low and a dangling bond carries out [an effect] termination, and the hydrogen pressure force returned oxygen from the silicon oxide which the hydrogen pressure force is too high in the hydrogen pressure force being more than an ordinary pressure (1.01x105Pa) again, for example, is used as a gate insulator layer, reduced the membraneous quality of an oxide film and caused the fall of a dielectric breakdown voltage, the hydrogen pressure force was made into the range of 0.1Pa - 1.01x105Pa
[0016] Moreover, hydrogen annealing by this invention can be performed in mixed-gas atmosphere with inert gas, such as the others, hydrogen and inert gas in hydrogen gas especially nitrogen, an argon, and helium.
[0017] in this case, hydrogen concentration is too low in the pressure of gas atmosphere being fixed to an ordinary pressure (1.01x105Pa), and the hydrogen concentration (hydrogen flow rate/(hydrogen flow rate + inert gas flow rate)) in mixed gas being below 0.5 %, and a dangling bond carries out termination -- it is ineffective and hydrogen concentration was made into 0.5% - 100% of range.
[0018] Furthermore, since annealing time was too short in hydrogen annealing time being 10 or less seconds, and could not fully carry out the termination of the dangling bond, and the oxygen of the silicon oxide too long [in annealing time being 3 hours or more / annealing] and used as a gate insulator layer was returned, the membraneous quality of an oxide film deteriorated and the fall of a dielectric breakdown voltage was caused, annealing time was made into the range of 10 seconds - 3 hours.
[0019]
[Example] Hereafter, the example of this invention is shown.
The sacrifice oxide film was formed after the usual RCA washing, and the 18 degree OFF 4 H-SiC EPI substrate (0001) (Si side, n type, Nd-Na=1x1016-/cm3) of examples was removed by HF. Subsequently, after forming a 36nm - 50nm oxide film by dry oxidization at 1100 degrees C, it quenched from 1100 degrees C to the room temperature. Then, temperature was changed to 400 degrees C - 1000 degrees C, and hydrogen annealing was performed for 30 minutes. The hydrogen pressure force was 5.6x103Pa at 1000 degrees C. Finally aluminum was used for the gate electrode and the ohmic contact, and the MOS capacitor was produced.
[0020] It is hydrogen annealing in the RF (f= 100kHz) valve flow coefficient property which drawing 1 is the cross section showing typically the MOS capacitor obtained in the example 1, and measured drawing 2 using this MOS capacitor.
[0021] valve flow coefficient and IV property are measured on condition that darkness in the box of the shielded metal, and the dashed line of the left-hand side in drawing 2 is an ideal curve calculated from the oxide-film capacity of 25V, and Nd-Na=1x1016-/cm3. A right-hand side dashed line is a valve flow coefficient characteristic curve when not carrying out hydrogen annealing, and the solid line inserted with the right-hand side dashed line and the left-hand side dashed line is a valve flow coefficient characteristic curve at the time of carrying out hydrogen annealing from right-hand side, respectively at 400 degrees C, 500 degrees C, 600 degrees C, 700 degrees C, and 1000 degrees C.
[0022] Among drawing, the thing with the actually measured value lower than the calculated value when a gate voltage is lower than -5V has very few minority carriers generated at a room temperature for the wide gap of 4 H-SiC, and it is because it will not be in equilibrium.
[0023] moreover, valve flow coefficient characteristic curve (right-hand side dashed line) when not carrying out hydrogen annealing -- setting -- a flat-band-voltage shift -- 15.7V -- very much -- large -- going and return of a gate voltage -- about 1 -- the hysteresis of V is shown and this means that there is very much interface level density
[0024] In valve flow coefficient characteristic curve of the solid line inserted with the right-hand side dashed line and the left-hand side dashed line, although a flat-band-voltage shift decreases when hydrogen annealing is carried out at 400 degrees C - 500 degrees C, since the value is large and a hysteresis is also large, it cannot still be used in fact.
[0025] On the other hand, when hydrogen annealing is carried out at 600 degrees C, a hysteresis disappears mostly, and when it is in the state where it can actually be used and hydrogen annealing is carried out at 1000 degrees C, a hysteresis disappears and approaches an ideal curve.
[0026] In addition, although a hysteresis disappearing completely and approaching an ideal curve further was expected when hydrogen annealing was carried out above 1000 degrees C, since the melting point of the silicon oxide currently generally used as a gate insulator layer was 1600 degrees C, the range of an annealing temperature was made into 600 degrees C - 1600 degrees C.
[0027]
[Effect of the Invention] Above, in short, according to this invention, interface level density can fully be reduced and good insulator layer / silicon-carbide interface which is fully equal to actual use can be acquired by carrying out termination of the silicon which exists in a gate insulator layer / silicon-carbide interface, or the carbonaceous tangling bond from hydrogen.

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Traci A. Brown

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